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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/822,669

04/13/2004

Se-young Jang

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21171 7590 07/11/2007  
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EXAMINER

DOAN, THERESA T

ART UNIT

PAPER NUMBER

2814

MAIL DATE

DELIVERY MODE

07/11/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/822,669	JANG ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 April 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4 and 7-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 7-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

1. The amendment filed on 04/089/07 has being acknowledged. By this amendment, claims 1-4, and 7-10 are pending in the application.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shi et al. (U.S. 6,746,896) in view of Admitted Prior Art (APA) as previously cited.

Regarding claim 1, Shi (Fig. 2) discloses a method of surface-mounting semiconductor chips on a PCB, including mounting a flip chip type semiconductor chip on the PCB consisting essentially of: forming a solder bump on a conductive contact area of each semiconductor chip on a back of a semiconductor wafer 100 mounted with a plurality of semiconductor chips (Fig. 2, column 5, lines 6-9); injecting underfill material on the area of the semiconductor wafer 100 formed with the solder bump 110 (Fig. 2, column 5, lines 9-16); hardening the underfill material partially to have a cohesive property (column 5, lines 15-16 and lines 33-67); severing the semiconductor wafer into the plurality of the semiconductor chips (column 5, lines 20-30); arranging the severed semiconductor chips having the hardened underfill material on the PCB (Fig. 2,

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column 5, lines 29-32); and heating the PCB at a predetermined temperature (column 5, lines 33-36).

Shi (Fig. 2) discloses a method of surface-mounting semiconductor chips on a PCB, including mounting a flip chip type semiconductor chip on the PCB, but fails to disclose a flip chip type semiconductor chip on the PCB mounted with electronic components.

However, APA (Fig. 2) shows that a PCB 400 is mounted with a semiconductor chip 200 and other electronic components 300 (see Background of the invention, paragraph [0007], lines 2-4) in a desired electronic application. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to mount the flip chip type semiconductor chip of Shi on the PCB mounted with electronic components in order to electrically connect the semiconductor chip to the electronic components in a desired electronic application, as taught by APA.

Regarding claim 2, Shi discloses that the predetermined heating temperature is above the temperature of a melting point of the solder bump (column 6, lines 8-11).

Regarding claim 3, Shi (Fig. 2) discloses that the underfill material is solidified during the heating (column 5, lines 15-16 and column 6, lines 19-21).

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4. Claims 4, and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shi et al. (U.S. 6,746,896) in view of Farnworth (U.S. 6,881,607) as previously cited.

Regarding claim 4, Shi (Fig. 2) discloses a process of preparing a wafer to be used for surface mounting a semiconductor chip on a PCB consisting essentially of: forming a plurality of solder balls 110 on a surface of a semiconductor wafer 100 (Fig. 2, column 5, lines 6-9); coating the surface of the semiconductor wafer formed with the solder balls 110 with underfill material (column 5, lines 9-16); curing the underfill material (column 5, lines 33-67); severing the semiconductor wafer into the plurality of semiconductor chips (column 5, lines 20-30); arranging the plurality of semiconductor chips on the PCB (column 5, lines 29-32); and raising the temperature of the PCB to a predetermined temperature (column 5, lines 33-36), wherein a temperature to cure the underfill material to a semisolid state is lower than a reflow temperature of the solder balls (column 6, lines 8-11).

Shi does not disclose a step of curing the underfill material to achieve a semisolid state.

However, Farnworth (Figs. 9-11) teaches a method for underfilling and encapsulating flip-chip configured semiconductor device mounted on a carrier substrate to form semisolid dam structure of photopolymeric material to entrap liquid (see Abstract) by using the laser light beam 112 to cure liquid resin 60 to at least a semisolid state (column 14, lines 42-45). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the process of

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Shi by performing a step of curing the underfill material to achieve a semisolid state because such curing the underfill material would provide a void-free dielectric underfill structure, as taught by Farnworth (column 5, lines 26-29).

Regarding claim 7, Shi discloses that the predetermined temperature is above the reflow temperature of the solder balls (column 6, lines 8-11).

Regarding claim 8, Shi discloses that the underfill is cured to a solid state at the predetermined temperature (column 5, lines 15-16).

Regarding claim 9, Shi discloses that the height of the underfill coating is approximately equal to the height of the solder balls (see Fig. 2).

Regarding claim 10, Farnworth (Fig. 11) discloses that the height of the underfill coating 60 is above the height of the solder balls 30.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-4 and 7-10 have been considered.

5. Applicant argues that the Shi reference does not suggest the invention as claimed because the transitional phrase "consisting essentially of" would limit the claim that the middle step of placing severed semiconductor chips on the carrying film, which is not required.

This argument is not persuasive because it is noted that the transitional phrase "consisting essentially of" limits the scope of a claim to the specified materials or steps "and those that do not materially affect the basic and novel characteristic(s)" of the claimed invention. *In re Herz*, 537 F.2d 549, 551-52, 190 USPQ 461, 463 (CCPA 1976). In this case, because there was no evidence that the presence of a step of placing severed semiconductor chips on the carrying film would materially affect the basic and novel characteristic of the claimed invention; the middle step of placing severed semiconductor chips on the carrying film would not be excluded from the scope of the claim. It is also noted that when an applicant contends that additional steps or materials in the prior art are excluded by the recitation of "consisting essentially of," applicant has the burden of showing that the introduction of additional steps or components would materially change the characteristics of applicant's invention. *In re De Lajarte*, 337 F.2d 870, 143 USPQ 256 (CCPA 1964). See also *Ex parte Hoffman*, 12 USPQ2d 1061, 1063-64 (Bd. Pat. App. & Inter. 1989).

The rest of applicant's arguments have been addressed and considered in the rejections shown above.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday, Tuesday and Thursday from 7:00AM - 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you



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have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T.D

July 8, 2007.

A handwritten signature in black ink, appearing to read "Theresa Doan", with a stylized, flowing script.

**THERESA DOAN  
PRIMARY PATENT EXAMINER**